TECHNICAL DATASHEET

Per Vices Corporation
High Performance SDR for Global Navigation Satellite Systems

Per Vices Corporation

Configuration: maximum dynamic range, 5MHz bandwidth, at specified frequency
Performance specifications are typical for measurements made within 50MHz of the specified frequency

TECHNICAL SPECIFICATIONS	GPS L1 @1227MHz	GPS L2 @1575MHz
Dynamic range (dB)	65	65
High Dynamic Range Option (Note 1)	110	110
Typical Rx noise figure (dB) (see Note 1)	1.2	1.4
Max Tx output power (dBm) (see Note 1)	15	15
Receiver sensitivity (dBm) (See Note 1)	-105	-105
Frequency tuning range (See Note 1)	100kHz to 18GHz	
	Supports all GPS, GALILEO, GLONASS, and BEIDOU bands	
Tuning time between different frequencies (see Note 2)	2ms	
Fast tuning time between frequencies (see Note 2)	40 µ	
Storage temperature	0-40 C	
Operating temperature	5-40 C	
Number of FPGA logic elements	350k (Crimson) / 2800k (Cyan)	
Peak floating-point performance (# of TFLOPS)	9.2 (Cyan)	
API documentation	Yes	
Antenna interface (see Note 1)	50Ω SMA	
Data interface (see Note 1)	SFP+ (10GBA SE-R) (Crimson) / qSFP+ (Cyan)	
Management interface (see Note 1)	RJ45	
MTBF (see Note 3)	23.6k hrs @ 40degC	
Volume (See Note 4)	19 inch server rack: 1U (Crimson) / 3U (Cyan)	
Mass	8kg (Crimson) / 11kg (Cyan)	
# of receive channels	0-16	
# of transmit channels	0-16	
Receive instantaneous bandwidth at FPGA	Up to 1GHz per channel	
Transmit instantaneous bandwidth at FPGA	Up to 1GHz per channel	
ADC resolution	16 bit	
DAC resolution	16 bit	
ADC sampling rate	up to 320MSPS (Crimson) / up to 1GSPS (Cyan)	
DAC sampling rate	up to 320MSPS (Crimson) / up to 1GSPS (Cyan)	
Frequency resolution	0.0625 Hz	
Frequency accuracy	2ppm (Crimson) / 50 ppb (Cyan)	
Adjustable pulse width	Available	
Real time kernal option	Available	

Note 1: This parameter may be adjusted to customer requirements.
Note 2: Product supports fast tuning times between frequencies that are integer multiples of one other. Arbitrary frequencies may take longer.
Note 3: Mean time between failure is calculated assuming sustained operation at environmental limits, and includes any single source of failures, including fans.
Note 4: The form factor may be optimized to accommodate SWaP requirements.

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INTERNAL ARCHITECTURE

The Digital board hosts the FPGA to manage communications with the host computer, in addition to in-unit DSP for quick response. Our standard radio chassis can have up to sixteen boards – some used for receiving data (Rx) and others used for transmitting data (Tx). With the coordination of a time board, the Rx and Tx boards receive inputs from the digital board through high speed interfaces, allowing the boards to be tuned to a new frequency within a couple of milliseconds (40 microseconds for fast tuning). The other end of the boards are attached to separate 50 Ohm SMA connectors. To transmit a digitally processed signal it is first sent to the DAC (digital-to-analog converter). The analog signal is then amplified and filtered for better transmission. When receiving an analog signal, it is first isolated with either a high-pass, low-pass or band-pass filter before being sent to the ADC for digitizing. The board's radio front end (RFE) can be used to control the aliasing, attenuation levels and gain characteristics of the analog signal.

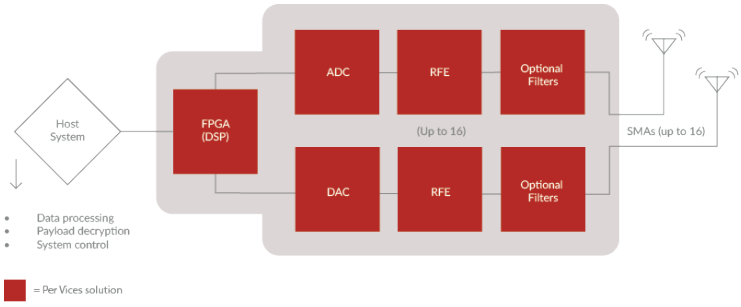
SDR INTEGRATION

The Tx/Rx boards can be programmed independently using either the internal reference crystal or with an external timing trigger. The boards have a 100kHz to 18GHz tuning range, allowing them to support various GNSS constellations, e.g. GPS, GALILEO, GLONASS, and BEIDOU bands (L1/ L2/L5, G1/G2, B1/B2, E1/ E5/E6, etc). When operating radios in congested or contested environments, our interface rejection and RF interference protection techniques allow for easy filtering and channel rejection, even if the channels are adjacent. The Cyan radio has a low noise figure and minimum detectable signal, making it possible to track onto weaker signals.

INTEGRATION CAPABILITIES

- API Documentation
- Antenna Interface
- Data Interface
- Management Interface
- FPGA Logic Elements
- Performance under contested environments
- Volume
- Mass

GNSS APPLICATION BLOCK DIAGRAM



PRODUCTION CAPABILITIES

Per Vices scales low, medium, and high volume capabilities to match the size of your project. Our build-your-own SDR tool allows you select from a wide range of features and certifications. The tool will also provide a rough order of magnitude (ROM) estimate. For more information or if you have more niche requirements, contact us directly and we'll help you out. We provide guaranteed performance on all our SDRs with standard factory test reports and customer specified reports.

EVALUATION REQUIREMENTS

Get started quickly with our COTS solutions, before proceeding with any optimizations required. This will allow you to use one of our stock products with a host system and UHD compatibility to demonstrate proof of concepts (POCs) and reduce overall risks associated with your project.

CONTACT US

More information is available at www.pervices.com.
If you have any questions, please contact us at solutions@pervices.com.

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