TECHNICAL DATASHEET

Per Vices Corporation
High Performance Software Defined Radio for Radar Systems

Per Vices has robust and flexible options to fit with your system requirements: Crimson TNG, Cyan, or a custom solution.

Settings: maximum dynamic range, 5MHz bandwidth, at specified frequency

TECHNICAL SPECIFICATIONS	L	S	C	X	Ku
	@1100MHz	@2800MHz	@5600MHz	@10000MHz	@18000MHz
Dynamic range (dB)	64	64	60	60	60
Typical Rx noise figure (dB) (see Note 1)	1.2	1.4	2	2	2.5
Max Tx output power (dBm) (see Note 1)	15	15	12	10	10
Receiver sensitivity (dBm) (see Note 1)	-150	-150	-104	-104	-103
Frequency tuning range	100 kHz to 18 GHz				
Tuning time between different frequencies (see Note 2)	2ms				
Fast tuning time between frequencies (see Note 2)	40us				
Storage temperature	0-40 C				
Operating temperature	5-40 C				
Number of FPGA logic elements	350k (Crimson) / 2800k (Cyan)				
Peak floating-point performance (# of TFLOPS)	9.2 (Cyan)				
API documentation	Yes				
Antenna interface (see Note 1)	50Ω SMA				
Data interface (see Note 1)	SFP+ (10GBA SE-R) (Crimson) / qSFP+ (Cyan)				
Management interface (see Note 1)	RJ45				
MTBF (see Note 3)	23.6k hrs @ 40degC				
Volume (See Note 4)	19 inch server rack: 1U (Crimson) / 3U (Cyan)				
Mass	8kg (Crimson) / 11kg (Cyan)				
# of receive channels	0-16				
# of transmit channels	0-16				
Receive instantaneous bandwidth at FPGA	Up to 1GHz per channel				
Transmit instantaneous bandwidth at FPGA	Up to 1GHz per channel				
ADC resolution	16 bit				
DAC resolution	16 bit				
ADC sampling rate	up to 320MSPS (Crimson) / up to 1GSPS (Cyan)				
DAC sampling rate	up to 320MSPS (Crimson) / up to 1GSPS (Cyan)				
Frequency resolution	0.0625 Hz				
Frequency accuracy	2ppm (Crimson) / 50 ppb (Cyan)				
Adjustable pulse width	Available				
Real time kernal option	Available				

Note 1: This parameter may be adjusted to customer requirements.
Note 2: Product supports fast tuning times between frequencies that are integer multiples of one other. Arbitrary frequencies may take longer.
Note 3: Mean time between failure is calculated assuming sustained operation at environmental limits, and includes any single source of failures, including fans.
Note 4: The form factor may be optimized to accommodate SWaP requirements

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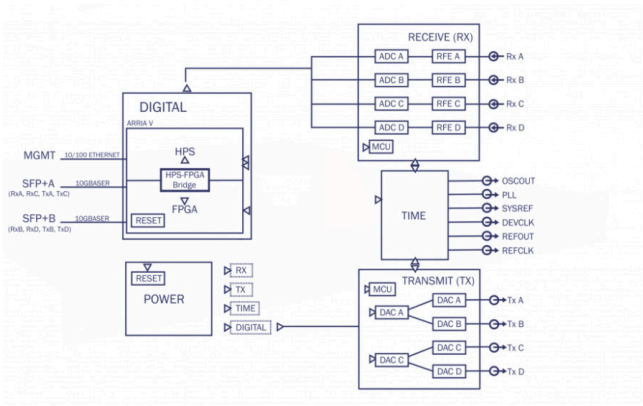
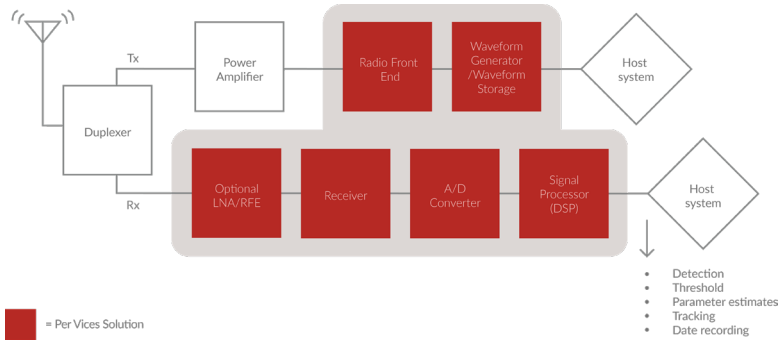
PER VICES RADAR SDR ARCHITECTURE



RADAR APPLICATION BLOCK DIAGRAM



INTERNAL ARCHITECTURE

The Digital board hosts the FPGA to manage communications with the host computer in addition to in-unit DSP for quick response. The Digital board sends data to DACs on the Transmit board, and receives data from the ADCs on the Receive board through high speed interfaces. The Time board distributes clock signals to all boards, from either internal reference crystal or user provided reference through a 50 Ohm SMA. The Power board distributes power to all boards from a Power Supply Unit compatible with 120V or 240V AC input.

INTEGRATION CAPABILITIES
API Documentation
Antenna Interface
Data Interface
Management Interface
FPGA Logic Elements
TFLOPS
Volume
Mass

EVALUATION REQUIREMENTS

Get started quickly with our COTS solutions, before proceeding to fully integrated solutions. This will allow you to use one of our stock products with a host system and UHD compatibility to demonstrate proof of concepts (POCs) and reduce overall risks associated with your projects.

SDR INTEGRATION

50 Ohm SMA RF interfaces, 10GBase-R or 40GBase-R data interfaces, and RJ45 Management interface may all be adjusted to suit user requirements for easy integration into existing or new systems. Provide external trigger for timing or synchronization via 50 Ohm SMA, which may be adjusted to suit user requirements. Trigger may be used in combination with wave-forms stored on the SDR. Per Vices SDRs accept or provide high precision timing for systems, through network or GPS PPS interfaces. Transmit and receive operations may be started based on time, rather than trigger signal. Further reduce system complexity by moving DSP and other computations from other devices onto the SDR FPGA. The radio may be configured to user SWaP requirements.

PRODUCTION CAPABILITIES

After the product has been integrated into your system, we offer full support through the lifetime of your project to ensure changes are not required. We guarantee performance with standard factory test reports and customer specified reports. Per Vices sales low, medium, and high volume capabilities to match the size of your project.

CONTACT US

More information is available at www.pervices.com.
If you have any questions, please contact us at solutions@pervices.com.

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